FALL PROCESSOR FORUM
www.in-stat.com/fpf

Tuesday
October 25, 2005
Doubletree Hotel
San Jose, CA

Premier sponsor:

IBM

Participating sponsors:

ARC

freescale semiconductor

Power.org

Media sponsors:

ElectronicNews

Electronic BUSINESS

InsideChips.com

semiconductor INTERNATIONAL

FPF Conference Program

TUESDAY OCTOBER 25, 2005

9:00 AM **Welcome and Intro**
Frank Dickson, Senior Director, In-Stat

9:05 AM **Keynote:** *Mike Fister, President & CEO, Cadence*

9:50 AM **Session One:** Multicore Processors
Kevin Krewell, Editor in Chief, MPR

A Concurrent Multi-Threaded Core for Complex SoCs
Kimming So, Senior Principal Scientist, Broadcom Corporation

SPARC64 VI/VI+: Fujitsu's Next Generation Processor
Takumi Maruyama, Manager of Enterprise Server Development, Fujitsu, Limited

10:45 AM Break (25 minutes)

The IBM PowerPC 970MP A New, Low-Power, High-Performance, Dual-Core Processor, *Norman J. Rohrer, Distinguished Engineer, IBM Corporation*

Application Customized CPU Design for Microsoft XBOX 360
Jeffrey D. Brown, Chief Engineer – Microsoft CPU Project, IBM Corporation

A Power-Efficient, Scalable Processor Family
Jim Keller, V. P. Engineering, Architecture Group, P. A. Semi

12:25 PM **Lunch** (80 minutes)

Special presentation: A Game Changing Innovation,
Scott Sellers, Co-founder, CTO & V. P. of Hardware Engineering, Azul Systems

2:15 PM **Session Two:** Innovative IP
Tom R. Halfhill, Senior Analyst

ARM's First Low-Power Superscalar Processor
David Williamson, Co-Architect and Validation Lead, ARM

Z-Ram and the Cinderella Effect
Mark-Eric Jones, President & CEO, Innovative Silicon, Inc.

3:10 PM Break (25 minutes)

3:35 PM **Session Three:** Processor IP for Multicore
Tom R. Halfhill, Senior Analyst

ARC's New Multi-Standard Multimedia Subsystem
Nigel Topham, Chief Architect, ARC International

High-Performance Multicore Video Decoder Technology Preview,
Gulbin A. Ezer, Hardware Design Manager, Tensilica

A Next-Generation Scalable Video Processor Core
Hans-Joachim Stolberg, CEO, videantis GmbH

5:30 PM Adjourn to Expo

FALL PROCESSOR FORUM

www.in-stat.com/fpf

Wednesday
October 26, 2005
Doubletree Hotel
San Jose, CA

Premier sponsor:

IBM

Participating sponsors:

ARC

freescale semiconductor

Power.org

Media sponsors:

ElectronicNews

Electronic BUSINESS

InsideChips.com

semiconductor INTERNATIONAL

WEDNESDAY OCTOBER 26, 2005

9:00 AM	Welcome
9:05 AM	**Keynote:** *Herb Sutter, Software Architect, Microsoft Developer Division*
9:50 AM	**Session Four:** Building Systems with Multicore Processors *Jim McGregor, Principal Analyst & Kevin Krewell, Editor in Chief, Microprocessor Report* Facing the Software Challenges of Multicore Designs *Neil Puthuff, Director of Hardware Engineering, Green Hills Software, Inc.*
10:35 AM	Break (20 minutes)
10:55 AM	Xen and the Art of Multicore Processing *Simon Crosby, V. P. of Strategy & Corporate Development, Xensource* AMD "Pacifica" Technology: x86 Architectural Enhancements to Facilitate Virtualization *Kevin McGrath, AMD Fellow*
12:15 PM	**Lunch** (75 minutes)
1:30 PM	Session Four continues Useable Multicore Implementations in Embedded Applications *Toby Foster, System Architect, Freescale Semiconductor* The Power Within the Cell Processor – and How to Unleash It *Alex Chow, Manager, S-T-I Design Center and David Krolak, Development Engineer, IBM* Part One, Part Two
2:50 PM	Break (20 minutes)
3:10 PM	**Session Five:** High Performance DSP *Max Baron, Principal Analyst* StarCore V5 Architecture *Amnon Rom CTO, V. P. Engineering, StarCore LLC* TMS320C672x DSP for Audio Processing, *Amitabh Menon, CPU and SoC Architect, Texas Instruments*
4:05 PM	**Session Six:** On Chip Interconnect for Multicore *Tom R. Halfhill, Principal Analyst* GALS Interconnect: Delivering Transparent Connectivity for Multi-Core SoCs *Uri Cummings, V. P. of Product Development, Fulcrum Microsystems* Advanced Dataflow Services for Heterogenious Multicore SoCs *Drew Wingard, CTO, Sonics*
5:00 PM	Adjourn